What is claimed is:

1. A memory system comprising:

a memory controller connected to at least one channel;

memory devices connected to the at least one channel, wherein at least one of the memory devices is a low bandwidth device being individually incapable of communicating a first data block with the memory controller during a first time period;

wherein the memory controller is configured to communicate control information to at least a first plurality of the memory devices via the at least one channel, and the first plurality of memory devices, as a multiplexed group on the channel, are configured to communicate a first data block between the memory controller and the first plurality of the memory devices during a first time period in response to the control information.

2. The memory system of claim 1, wherein each one of the first plurality of memory devices is configured to contribute a second data block, less than the first data block, to the first data block communicated during the first time period.

3. The memory system of claim 2, wherein the at least one channel comprises two channels, each one of the two channels connecting a second plurality of memory devices to the memory controller.

4. The memory system of claim 3 wherein the second plurality of memory devices comprises sixteen memory devices.

5. The memory system of claim 2, wherein the at least one channel comprises four full channels and one half channel, each one of the full channels connecting a second plurality of memory devices, and the one half channel connecting half the second plurality of memory devices.

6. The memory system of claim 5, wherein the second plurality of memory devices comprises sixteen memory devices.

7. The memory system of claim 2, wherein the at least one channel comprises eight channels, each channel connecting a second plurality of memory devices.

8. The memory system of claim 7, wherein the second plurality of memory devices comprises eight memory devices.

9. The memory system of claim 2, wherein the at least one channel comprises four channels, each channel connecting a second plurality of memory devices.

10. The memory system of claim 9, wherein the second plurality of memory devices comprises eight memory devices.

11. A memory system comprising:

a memory controller connected to at least one repeater via a main channel;

wherein each repeater connects a first plurality of memory devices via at least one auxiliary channel, and wherein each one of the first plurality of memory devices is a low bandwidth device individually incapable of communicating a first data block with the memory controller during a first time period;

wherein the memory controller is configured to communicate control information to the first plurality of the memory devices via the at least the main channel, the at least one repeater, and the at least one auxiliary channel, and the first plurality of memory devices, as a multiplexed group on the channel, are configured to communicate a first data block between the memory controller and the first plurality of the memory devices during a first time period in response to the control information.

12. The memory system of claim 11, wherein each memory device in the first plurality of memory devices contributes a second data block, less than the first data block, to the first data block transferred during the first time period.

13. The memory system of claim 11, wherein the at least one repeater connects a second plurality of memory devices via a first auxiliary channel, and connects a third plurality of memory devices via a second auxiliary channel.

14. The memory system of claim 13, wherein each one of the second and third pluralities of memory devices comprises eight memory devices.

15. A memory system capable of selectively operating in first and second modes, comprising:

a memory controller, memory devices, and a channel connecting the memory controller with the memory devices;

wherein each one of the memory devices is capable of operating in at least a first and a second power state, the first power state consuming more power than the second power state; such that

while the memory system is operating in the first mode, the memory controller is configured to generate a first power down device identification (ID) unique to one of the memory devices, whereby the one memory device upon receiving the first power down device ID will transition from the first power state to the second power state; and

while the memory system is operating in the second mode, the memory controller generates a second power down device ID having the same structure as the first power down device ID, such that a plurality of memory devices upon receiving the second power down device ID transition from the first power state to a second power state.

16. A method of reading data in a memory system during a first time period, the memory system comprising a memory controller connected to memory devices via a data bus having multiple data bus lines, the method comprising:

communicating at least one command packet from the memory controller to a plurality of the memory devices;

for each memory device in the plurality of memory devices, seizing at least one data bus line during the first time period and returning data to the memory controller via the at least one data bus line in response to the at least one command packet.

17. The method of claim 16, wherein the first time period comprises a sequence of second time periods, and wherein each memory device in the plurality of memory devices seizes at least one data bus line during each one of the second time period.

18. The method of claim 17, wherein the data bus implements a wired OR function.